What is claimed is:

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1 1.	An output stage	for a	differential	amplifier	comprising:
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- first and second P-type input amplifiers to receive a non-inverted differential voltage signal and an inverted differential voltage, respectively;
 - first and second N-type input amplifiers to receive the non-inverted differential voltage signal and the inverted differential voltage, respectively;
 - a first output amplifier to receive the output of the first P-type input amplifier via an N-type load and the output of the first N-type amplifier via a P-type load; and
 - a second output amplifier to receive the output of the second P-type input amplifier via an N-type load and the output of the second N-type amplifier via a P-type load.
 - 2. The output stage of claim 1 wherein an output voltage signal is to be provided between said first and second output amplifiers.
 - 3. The output stage of claim 2 wherein said first output amplifier is a P-type amplifier and said second output amplifier is an N-type amplifier.
- 1 4. The output stage of claim 1 wherein said non-inverted differential voltage signal and said 2 inverted differential voltage signal have matched currents.
- 1 5. An output stage for a differential amplifier comprising:
- first and second P-type transistors to receive a non-inverted differential voltage and an inverted differential voltage, respectively;

4		first and second N-type transistors to receive the non-inverted differential voltage and the			
5	inverted differential voltage, respectively;				
6		a first output amplifier to receive the output of the first P-type transistor via an N-type			
7	load and the output of the first N-type transistor via an N-type load; and				
8		a second output amplifier to receive the output of the second P-type transistor via an N-			
9	type lo	oad and the output of the second N-type transistor via an N-type load.			
1	6.	The output stage of claim 5 wherein an output voltage is to be provided between said first			
2	and se	and second output amplifiers.			
	8.	The output stage of claim 6 wherein said first output amplifier is a P-type transistor and cond output amplifier is an N-type transistor. The output stage of claim 5 wherein said non-inverted differential voltage signal and said ad differential voltage signal have matched currents.			
1	9.	An output stage for a differential amplifier comprising:			
2		first and second P-type transistors to receive a non-inverted differential voltage and an			
3	inverte	ed differential voltage, respectively;			
4		first and second N-type transistors to receive the non-inverted differential voltage and the			
5	inverted differential voltage, respectively;				
6		first and second N-type loads coupled to said first and second P-type transistors,			

respectively;

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8		first and second P-type loads coupled to said first and second N-type transistors,			
9	respec	tively;			
10		first and second intermediate transistors coupled to said first P-type transistor and said			
11	first N	-type transistor;			
12		a first output amplifier to receive the output of the first intermediary transistor and the			
13	output of the second N-type transistor; and				
14		a second output amplifier to receive the output of the second intermediary transistor and			
15	the ou	tput of the second P-type transistor.			
	10.	The output stage of claim 9 wherein an output voltage is to be provided between said first cond output amplifiers.			
	11.	The output stage of claim 10 wherein said first output amplifier is a P-type transistor and econd output amplifier is an N-type transistor.			
	12.	The output stage of claim 11 wherein said first intermediary transistor is a P-type			
2	transis	stor and said second intermediary transistor is an N-type transistor.			
1	13.	The output stage of claim 9 wherein each of said transistors is a metal-oxide-			
2	semiconductor field effect transistor.				

14. The output stage of claim 7 wherein said non-inverted differential voltage signal and said inverted differential voltage signal have matched currents.

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- 1 15. The output stage of claim 12 wherein said non-inverted differential voltage signal and
- 2 said inverted differential voltage signal have matched currents.